

Amendments to the claims:

This listing of the claims will replace all prior versions and listings of the claims in the application:

Listing of Claims:

1. (Currently Amended) An electrical device (200) for efficient and flexible control of memory access, ~~said device (200) being~~
~~connected to at least one memory accessing unit (202), and~~
~~connected to a memory (100) comprising at least one physical memory module (203),~~
~~said device (200) comprising the device comprising:~~

at least two access channel circuits (300), ~~where, wherein~~ at least one of the access channel ~~circuit (300) circuits~~ is connected to said at least one memory accessing unit (202) via at least one system bus (304; 308) and to said at least one physical memory module (203), ~~said of a memory, the~~ at least one access channel circuit (300) providing memory access for ~~said the~~ at least one memory accessing unit (202) to at least a part of ~~said the~~ memory (100).

2. (Currently Amended) An electrical device (200) according to claim 1, ~~characterized in that said~~ wherein the at least one memory accessing unit comprises a plurality of memory accessing units, and wherein the at least two access channel circuits (300) each provides memory access for at least one of the plurality of memory accessing ~~units unit~~ (202) to at least a part of the memory (100) thereby allowing the memory accessing units (202) connected to different access channel circuits (300) independent and simultaneous/parallel access to different parts of the memory (100).

3. (Currently Amended) An electrical device (200) according to ~~claims 1—2,~~
~~characterized in that said claim 1, wherein the device (200) further~~ comprises:

a control and configure circuit (201) configured to dynamically control ~~controlling~~ ~~said the~~ at least two access channel circuits (300), ~~said the~~ control and configure circuit (201) allowing for ~~simple~~ an addition of ~~further~~ additional access channel circuits (300) ~~during~~ implementation.

4. (Currently Amended) An electrical device (200) according to ~~claims 1—3~~, characterized in that ~~said device comprises claim 1~~, wherein the at least one memory accessing unit comprises a plurality of memory accessing units, and wherein the at least two access channel circuits (300) ~~each being~~ are each connected via ~~a single~~ the at least one system bus (304, 308) to ~~a single one of the plurality of memory accessing units unit (202)~~ and each of the at least two access channel circuits are ~~being~~ connected (210) to receive information/data from at least a part of ~~said the memory (100)~~.

5. (Currently Amended) An electrical device (200) according to ~~claims 1—4~~, characterized in that ~~said device (200) comprises one claim 1~~, wherein the at least one memory accessing unit comprises at least two memory accessing units, and wherein one of the at least two access channel circuit (300) circuits is connected via ~~a single~~ the at least one system bus (304, 308) to the at least two memory accessing units (202), ~~said the one of the at least two access channel circuit (300) circuits~~ being connected (210) to receive data/information from and/or transmit data/information to at least a part of ~~said the memory (100)~~.

6. (Currently Amended) An electrical device according to ~~claims 1—5~~, characterized in that ~~said an claim 1~~, wherein the at least one physical memory module comprises a first physical memory module and a second physical memory module, wherein at least one of the access channel circuit circuit (300) further comprises an automatic data transfer engine (301) for transferring data/information from ~~[[a]] the first physical memory module (203) of the memory (100) to [[a]] the second physical memory module (203) of the memory (100) prior to [[a]] the at least one memory accessing unit device (202) retrieving said the data/information.~~

7. (Currently Amended) An electrical device according to claim 6, ~~characterized in that~~ wherein each of the at least two access channel circuits comprises an automatic data transfer engines (301) of a plurality of access channel circuits (300) are engine, the automatic data transfer engines being connected to form a chain of automatic data transfer engines where each data transfer engine (301) is responsible for transferring a different part of ~~said the data/information.~~

8. (Currently Amended) An electrical device according to ~~claims 3—7~~, characterized in that ~~said at least one claim 3~~, wherein at least one of the access channel circuits (300) comprises at least one special purpose register and is connected (307) to ~~said the~~ control and configure circuit (204), ~~where said wherein the~~ control and configure circuit (204) is adapted to modify a content of ~~said the~~ at least one special purpose register thereby allowing for reconfiguration of ~~individual at least one of the~~ access channel circuits (300) without affecting ~~either another one of the~~ access channels (300) during an operation of the device.

9. (Currently Amended) An electrical device according to claim 8, ~~characterized in that said reconfiguration comprises wherein the~~ at least one special purpose register is adapted to reconfigure at least one of the access channel circuits by configuring a mode of functionality and/or at least one access region of said the memory (100).

10. (Currently Amended) An electrical device according to ~~claims 1—9~~, characterized in that ~~said claim 1~~, wherein the device (200) comprises has one access channel circuit (300) for each connected memory accessing unit (202) and ~~in that wherein~~ each access channel circuit (300) is connected with each memory module (203) of ~~said the~~ memory (100).

11. (Currently Amended) An electrical device according to ~~claims 1—10~~, characterized in that ~~an claim 1~~, wherein the at least one memory module comprises a plurality of memory modules and the at least one access channel circuit (300) comprises:

a memory access controller (301) adapted to monitor an incoming system bus (304), connected to ~~[[a]] one of the memory accessing units device (202)~~, and an outgoing system bus (308) connected to ~~[[a]] the memory accessing unit device (202)~~ for a first identifier representing a given memory bus (209) to be connected, the memory access controller (301) providing a first control signal/code, based on ~~said the~~ first identifier, representing ~~said the~~ given memory bus (209) and to where ~~said the~~ given memory bus (209) is to be connected,

a source and destination selector (303) for enabling access to a memory bus (209), connected to ~~[[a]] one of the memory modules module (203)~~ of ~~said the~~ memory (100), from ~~said the~~ incoming system bus (304) or ~~said the~~ memory access controller (301) dependent on ~~said the~~ first control signal/code received from ~~said the~~ memory access controller (301), and

a memory module selector (302) for selecting which of the memory modules module (203) is to be connected to the outgoing system bus (308), connected to said the memory accessing device (202), during a given read access of a specific memory module (203) one of the memory modules dependent on a second unique identifier.

12. (Currently Amended) A method of ~~efficient and flexible~~ control of memory access between at least one memory accessing unit (202) and a memory (100) comprising at least one physical memory module (203), the method comprising ~~the step of:~~

providing, ~~by~~ with at least one of at least two access channel circuits (300), memory access for said the at least one memory accessing unit (202) to at least a part of said the memory (100), ~~where said wherein the~~ at least one access channel circuit (300) is connected to said the least one memory accessing unit (202) via at least one system bus (304; 308) and to said the at least one physical memory module (203).

13. (Currently Amended) A method according to claim 12, ~~characterized in that said method comprises the step of wherein the~~ at least one memory accessing unit comprises at least two memory accessing units, the method further comprising:

providing simultaneous memory access for said the at least two memory accessing units (202) to at least a part of the memory (100) via said the at least two access channel circuits (300), each access channel providing independent access to different parts of the memory (100), thereby allowing the at least two memory accessing units (202) connected to different access channel circuits (300) parallel access to different parts of the memory (100).

14. (Currently Amended) A method according to ~~claims 12—13, characterized in that said claim 12, the method further comprising:~~ comprises the step of:

dynamically controlling said the at least two access channel circuits (300) ~~by~~ with a control and configure circuit (201), said the control and configure circuit (201) allowing for simple an addition of further additional access channel circuits (300) ~~during implementation.~~

15. (Currently Amended) A method according to ~~claims 12—14, characterized in that said claim 12, wherein the~~ at least one access channel circuit comprises at least two access channel circuits, the method further comprising: ~~comprises the step of:~~

providing memory access to ~~a single~~ the at least one memory accessing unit (202) from at least a part of ~~said~~ the memory (100) by with the at least two access channel circuits (300) each being connected via a ~~single~~ respective system bus (304, 308) to the ~~single at least one~~ memory accessing unit (202) and each being connected (210) to receive information/data from at least a part of ~~said~~ the memory (100).

16. (Currently Amended) A method according to ~~claims 12—15, characterized in that said method comprises the step of:~~ claim 12, wherein the at least one memory accessing unit comprises at least two memory accessing units, the method further comprising
providing memory access to the at least two memory accessing units (202) from at least a part of ~~said~~ the memory (100) by ~~a single~~ with the at least one access channel circuit (300) connected via a ~~single~~ system bus (304, 308) to ~~said~~ the at least two memory accessing units (202), ~~said single, the~~ access channel circuit (300) being connected (210) to receive data/information from and/or transmit data/information to at least a part of ~~said~~ the memory (100).

17. (Currently Amended) A method according to ~~claims 12—16, characterized in that said method further comprises the step of:~~ claim 12, wherein the at least one memory module comprises a first memory module and a second memory module, the method further comprising:

providing automatic data transfer of data/information ~~by an~~ with the access channel circuit (300), the access channel circuit comprising an automatic data transfer engine (301) for transferring data/information from ~~[[a]]~~ the first physical memory module (203) of the memory (100) to ~~[[a]]~~ the second physical memory module (203) of the memory (100) prior to ~~[[a]]~~ the memory accessing ~~unit device~~ (202) retrieving ~~said~~ the data/information.

18. (Currently Amended) A method according to claim 17, ~~characterized in that said comprises the step of:~~ wherein the automatic data transfer engine comprises a plurality of data transfer engines, and the access channel circuit comprises a plurality of access channel circuits, wherein

~~providing automatic data transfer of data/information where a~~ the plurality of automatic data transfer engines (301) of ~~[[a]]~~ the plurality of access channel circuits (300) are connected to form a chain of automatic data transfer engines and

where wherein each data transfer engine (301) is responsible for transferring a different part of said portion of the data/information.

19. (Currently Amended) A method according to ~~claims 14—18, characterized in that said method comprises the step of:~~ claim 14, further comprising:

modifying, ~~by said~~ with the control and configure circuit (201), a content of at least one special-purpose register, ~~comprised by wherein~~ at least one access channel circuit (300) of the at least two access channel circuits is connected (307) to said the control and configure circuit (201), thereby allowing for reconfiguration of ~~individual the at least one access channel circuit circuits (300) without affecting another one of the at least two access channel circuits other access channels (300) during an operation of the access channel circuits.~~

20. (Currently Amended) A method according to claim 19, ~~characterized in that said reconfiguration comprises further comprising~~ configuring a mode of functionality and/or at least one access region of said the memory (100).

21. (Currently Amended) A method according to ~~claims 12—20, characterized in that claim 12, wherein the at least one memory accessing unit comprises at least two memory accessing units and the at least one memory module comprises a plurality of memory modules, the method further comprising providing memory access is provided by one of the at least two access channel circuits access channel circuit (300) for each connected one of the at least two memory accessing units memory accessing unit (202) where each of the at least two access channel circuits access channel circuit (300) is connected with each of the plurality of memory modules memory module (203) of said the memory (100).~~

22. (Currently Amended) A method according to ~~claims 12—21, characterized in that said method further comprises the steps of:~~ claim 22, wherein the at least one memory accessing unit comprises a plurality of memory accessing units, the method further comprising:

monitoring, ~~by with~~ a memory access controller for a first identifier representing a given memory bus to be connected (301) comprised by, the memory access controller comprising the [[an]] access channel circuit (300), an incoming system bus (304), connected to [[a]] one of the memory accessing units memory accessing device (202), and an outgoing

system bus (308) connected to ~~another one of the memory accessing units~~ a memory accessing device (202) for a first identifier representing a given memory bus (209) to be connected,

providing, ~~by~~ with the memory access controller (301), a first control signal/code, based on said the first identifier[[,]] representing said the given memory bus (209) and to where said the given memory bus (209) is to be connected,

enabling access, ~~by~~ with a source and destination selector (303), to [[a]] another memory bus (209), connected to [[a]] one of the memory modules module (203) of said the memory (100), from said the incoming system bus (304) or said the memory access controller (301) dependent on said the first control signal/code received from said the memory access controller (301), and

selecting, ~~by~~ with a memory module selector (302), which of the memory modules module (203) is to be connected to the outgoing system bus (308), connected to said the memory accessing device (202), during a given read access of a specific one of the memory modules module (203) dependent on a second unique identifier.

23. ~~(Currently Amended) Use of an electrical device according to claims 1—11, characterized in that said~~ The electrical device of Claim 1, wherein the electrical device (200) is used provided in a mobile communications terminal (501).

24. ~~(Currently Amended) Use of a method according to claims 12—22, characterized in that said method is used in~~ The method of Claim 12, wherein the method is carried out by a mobile communications terminal (501).

25. (Canceled).